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Claims

1. A power amplifier circuit for amplifying an input RF signal with respect to a specified RF output power, comprising

- an input terminal (2) for supplying the input RF signal to be amplified,
- an output terminal for the RF signal with the output power specified,
- an amplification path (3) formed between the input terminal (2) and the output terminal (7) having a power amplification circuit (4) for amplifying the RF signal,
- a bypass (5) formed between the input terminal (2) and the output terminal (7) for the RF signal to bypass the amplification path (3),
- a control terminal (6) for controlling the operation of the amplification path (3) and the bypass (5) such, that an RF signal is either passed through the amplification path (3) or the bypass (5),

characterised by

- a variable gain amplifier circuit (15) for a pre-amplification of the input RF signal which is placed between the line from the input terminal (2) to the amplification path (3) and the bypass (5), and
- a delay control means (16, 17, 18, 19) for controlling the variable gain amplifier (15), the amplification path (3), and the bypass (5),

whereby, before setting the operating conditions of the variable gain amplifier (15), the amplification path (3), and the bypass (5) in a state to achieve the RF output power specified, the delay control means (16, 17, 18, 19) is adapted to first set the respective operating conditions in the inverse state thereof.

2. A power amplifier circuit according to claim 1, characterised in that the delay time period for which the delay control means (16, 17, 18, 19) sets the operating conditions of the variable gain amplifier (15), the amplification path (3), and the bypass (5) in the inverse state thereof corresponds to half the settling time (τ) for an RF output power change.

3. A power amplifier circuit according to claim 1 or 2,

characterised in

that the control means comprises a latch trigger circuit (16) for controlling the operation of the amplification path (3) and the bypass (5), a sample-and-hold circuit (17) for controlling the gain factor of the variable gain amplifier circuit (15), a digital multiplexer circuit (18) for selecting a control signal, and delay circuit (19) for delaying a control signal by the delay time period.

5 4. A power amplifier circuit according to anyone of the claims 1, 2 or 3,
characterised by

10 the bypass (5) comprising a first matching circuit (8), a second matching circuit (9), and a first controllable switch (10) for controllably adapting the impedance of the bypass to either block or open it for a passage of an RF signal.

15 5. A power amplifier circuit according to anyone of the claims 1 to 4,
characterised by

the amplification path (3) comprising a third matching circuit (14) and a controllable second switch (11) for controllably adapting the impedance of the amplification path (3) to either amplify an RF signal or block the passage for the RF signal.

20 6. A power amplifier circuit according to anyone of the claims 1 to 5,
characterised by

the control terminal (6) being adapted to provide control information to the delay control means (16, 17, 18, 19).

25 7. A power amplifier circuit according to anyone of the claims 3 to 6,
characterised by

the variable gain amplifier circuit (15) comprising a digital and/or analogue gain control.

30 8. A power amplifier circuit according to anyone of the claims 3 to 6,
characterised in

that the input RF signal is a signal coded for use in an UMTS communication system.

35 9. A mobile terminal for a wireless telecommunication system with a power amplifier circuit (1'') according to one of the claims 1 to 8.

10. A method for amplifying an input RF signal with respect to a specified RF output power, comprising the steps of

- supplying the input RF signal to be amplified,
- outputting the RF signal with the output power specified,
- 5 – amplifying the RF signal in an amplification path (3) formed between an input terminal (2) and an output terminal (7),
- selectively bypassing the amplification path (3),
- controlling the operation of the amplification path (3) and the bypass (5) such that an RF signal is either passed through the amplification path (3) or the bypass (5),

10 characterised by

- pre-amplifying the input RF signal by a variable gain amplifier circuit (15) which is placed between the line from the input terminal (2) to the amplification path (3) and the bypass (5), and
- 15 – controlling the variable gain amplifier (15), the amplification path (3), and the bypass (5) by a delay control means (16, 17, 18, 19),

whereby, before setting the operating conditions of the variable gain amplifier (15), the amplification path (3), and the bypass (5) in a state to achieve the RF output power specified, the respective operating conditions are at first set in the inverse state thereof via the delay control means (16, 17, 18, 19).

20 11. A method according to claim 10,

characterised by the step of

25 setting the operating conditions of the variable gain amplifier (15), the

amplification path (3), and the bypass (5) by the delay control means (16, 17, 18, 19) in the inverse state thereof for a delay time period that corresponds to half the settling time (τ) for an RF output power change.

30 12. A method according to claim 10 or 11,

characterised by the step of

35 controlling the operation of the amplification path (3) and the bypass (5) by a latch trigger circuit (16) integrated in the control means, controlling the gain factor of the variable gain amplifier circuit (15) by a sample-and-hold circuit (17), selecting a control signal by a digital multiplexer circuit (18), and delaying a control signal by the delay time period by a delay circuit (19).

35 13. A method according to anyone of claims 10, 11 or 12,

characterised by the step of

controllably adapting the impedance of the bypass to either block or open it for a passage of an RF signal by a first matching circuit (8), a second matching circuit (9), and a first controllable switch (10) integrated in the bypass (5).

5 14. A method according to anyone of the claims 10 to 13,
characterised by the step of
controllably adapting the impedance of the amplification path (3) to either amplify
an RF signal or block the passage for the RF signal by a third matching circuit (14)
and a controllable second switch (11) integrated in the amplification path (3).

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15. A method according to anyone of the claims 10 to 14,
characterised by the step of
adapting the control terminal (6) to provide control information to the delay control
means (16, 17, 18, 19).

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